AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [0036] with the following amended paragraph:

[0036] The acquisition group of switched capacitors is further divided into two subgroups: environmental and channel select. The environmental subgroup corrects the center oscillating frequency of the operational band due to process-voltage-temperature (PVT) variations and could be performed at manufacturing, on power-up or on "as needed" basis. The channel select capacitor array 14b controls the frequency acquisition process for the desired transmission channel. Both groups are best implemented using individual binary-weighted capacitance structures, but their ranges could be overlapping. There is no need to preserve the binary-weight continuity between the environmental and channel select structures due to the different origin of their respective control inputs. The PVT correction is infrequent and ~~and~~ might be done directly through register interface, whereas the channel select DCO control input is performed dynamically and is an integral part of the synthesizer PLL (phase locked loop).

Please replace paragraph [0040] with the following amended paragraph:

[0040] Figure 3 illustrates a block diagram of the tracking oscillator controllers 28 and 30. In the illustrated embodiment, the TUNE_T, the tuning word output from the phase detection[[s]] and gain circuit 36, has six integer bits and five fractional bits. The integer bits are processed by the integer tracking oscillator controller 28 and the fractional bits are processed by the fractional tracking oscillator controller 30. The integer tracking

oscillator controller 28 includes a row select circuit 40 and a column select and DEM (dynamic element matching) circuit 42. The outputs of the row select circuit 40 and a column select and DEM circuit 42 are received by a switch matrix 44. The switch matrix 44 provides sixty-four discrete switches 46 (corresponding to the sixty-four switched capacitors in the integer tracking array 14c) that may be enabled or disabled by the row select circuit 42 and column select and DEM circuit 42 responsive to TUNE_T. The switch matrix is coupled to a bank of sixty-four resampling drivers 48, each individual resampling driver 48 having a respective switch 46 and a respective capacitor 18 in switched capacitor array 14c. The resampling drivers 48 selectively enable or disable capacitors in the integer tracking array 14c in response to the associated switches 46. Using resampling drivers 48 clocked at CKR eliminates timing errors due to path differences. The various capacitor arrays 14a-d of the LC tank 12 are part of the DCO 49.

Please replace paragraph [0056] with the following amended paragraph:

[0056] Figure 12a illustrates a more detailed block diagram of the phase operation portion of the RF transmitter 10. The phase detector and gain circuit 36 includes individual PVT, acquisition and tracking gain circuits 52, 54 and 56 and a phase detection circuit 60. The phase error (PHE) output of the phase detector is received by the gain circuits 52-56 (each gain circuit uses an individual set of bits of PHE). The gain circuits 52-56 multiply the respective portions of PHE by an associated factor, GAIN_P, GAIN_A and GAIN_T. The outputs of the gain circuits, TUNE_P, TUNE_A and TUNE_T are the oscillator tuning words that control the oscillator control circuits 24, 26, 28 and 30. As described in greater detail above, the oscillator control circuits sequentially control the DCO 12 through start-up, acquisition and tracking phases.